

### REMARKS

Claims 1-18, 27-66, 70-78 and 80-84 are pending with claims 1-12 and 81 being independent. Claims 1-10, 13-18, 27-66, 70-78 and 80 have been withdrawn from consideration, leaving independent claims 11, 12 and 81, and their dependent claims 82-84, under consideration. Claims 67-69 have been canceled and claims 82-84 have been added. Support for the new claims may be found in the application at, for example, Figs. 3-3F and the associated text. No new matter has been introduced.

Initially, applicant thanks the Examiner for the personal interview granted to the undersigned on May 1. The substance of the interview is set forth below.

As discussed at the interview, on the information disclosure statement initialed as being considered on January 12, 2007, the Examiner has indicated that no abstract was provided for reference "CT" (JP3287391). However, applicant notes that JP3287391 was submitted with the abstract of JP11-040755, which is the laid open patent application number of JP3287391, and which is believed to have an abstract equivalent to that of JP3287391.

Claims 11, 12 and 81 have been rejected as being anticipated by Koyama (U.S. 2001/0048408 A1).

With respect to claims 11 and 12, applicant requests reconsideration and withdrawal of this rejection because Koyama does not describe or suggest a current source configured to receive a set signal and a signal current, and to control an output current value corresponding to the signal current, as recited in each of amended independent claims 11 and 12. For example, the storage circuit of Fig. 5B of Koyama, which the rejection equates with the recited current source, comprises an SRAM circuit that does not control an output current corresponding to an input signal current and, instead, sets an output potential based on an input potential.

At the interview, the Examiner indicated, in particular, that the gate transistors of Fig. 5B of Koyama (i.e., the elements which receive the input, control signal 1 and control signal 2) correspond to the recited current sources. However, as discussed at the interview, one of

ordinary skill in the art would not have understood a gate transistor such as is shown in Fig. 5B to constitute a "current source."

This distinction is further emphasized by new dependent claims 82 and 83, each of which recites that each of the current sources includes at least one switch and at least one transistor having a gate, with the switch being connected to control a voltage applied to the gate of the transistor. As noted above, the Examiner has indicated that a single gate transistor corresponds to a recited current source. However, a single gate transistor cannot be said to correspond to a switch and a transistor connected in the manner recited in claims 82 and 83.

Similarly to claims 11 and 12, independent claim 81 recites current source circuits, each of which is supplied a first current and supplies a second current corresponding to the first current. As noted above, one of ordinary skill in the art would not have understood a gate transistor such as is shown in Fig. 5B of Koyama to constitute a "current source circuit."

This distinction is further emphasized by new dependent claim 84, which recites that each of the current source circuits includes at least one switch and at least one transistor having a gate, with the switch being connected to control a voltage applied to the gate of the transistor. As noted above, the Examiner has indicated that a single gate transistor corresponds to a recited current source circuit. However, a single gate transistor cannot be said to correspond to a switch and a transistor connected in the manner recited in claim 84.

Accordingly, for at least these reasons, the rejection should be withdrawn.

Applicant : Hajime Kimura et al.  
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Filed : January 14, 2004  
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The fee in the amount of \$120 in payment of the one-month extension fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,



Date: May 22, 2007

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